

## Figures

The diagram shows a differential signal path. A horizontal line at the bottom is labeled WL1. Two vertical lines, BL1 and BL2, extend upwards from WL1. Transistor T1 is connected between BL1 and a common node. Transistor T2 is connected between BL2 and the same common node. The gates of T1 and T2 are connected to a common horizontal line. A capacitor C<sub>ref</sub> is connected between this common gate line and a top horizontal line. The top horizontal line is connected to two vertical lines, C<sub>ds1</sub> and C<sub>ds2</sub>. Dashed boxes indicate parasitic capacitance regions: C<sub>db1</sub> and C<sub>db2</sub> are connected to the gates of T1 and T2 respectively, and C<sub>sb1</sub> and C<sub>sb2</sub> are connected to the sources of T1 and T2 respectively.

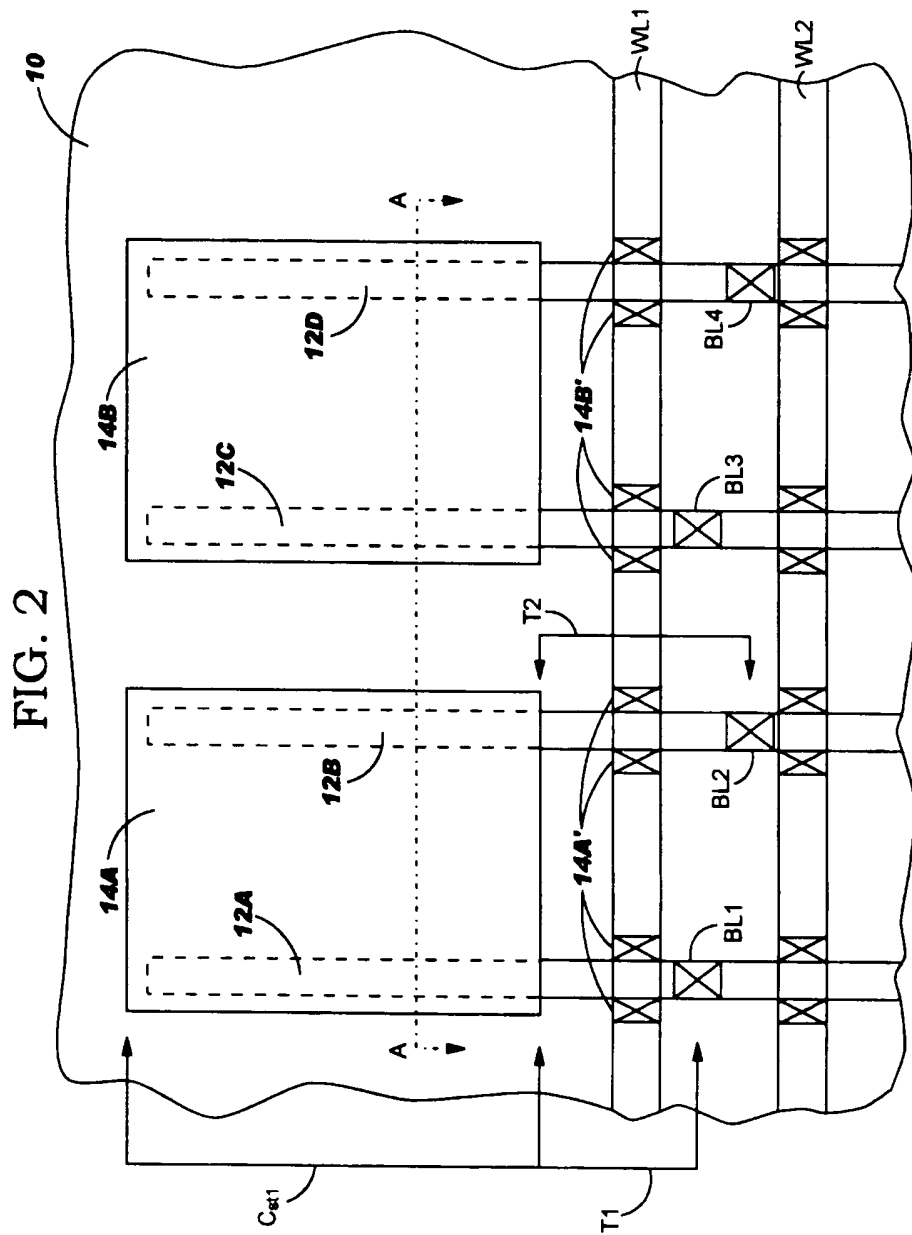


FIG. 3

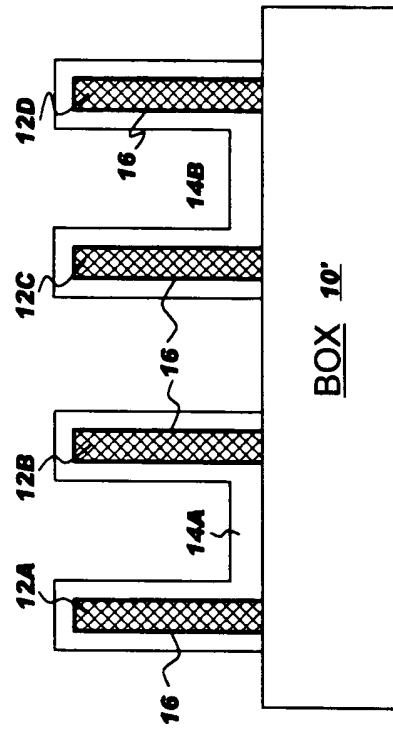


FIG. 4

